CLAIMS

What is claimed is:

1. An apparatus, comprising:

a daughter printed wiring board having a bottom surface and a top surface, and a plurality of electrical conductors extending from said bottom surface to said top surface; and

a substrate having a probe surface and a connector surface, said probe surface having a plurality of spring probe contact tips, said connector surface having a plurality of electrically conductive pads, a plurality of electrical connectors between each of said plurality of said spring probe contact tips and each of said plurality of electrically conductive pads, and a plurality of electrical connections between said plurality of electrically conductive pads and said plurality of electrical conductors on said bottom surface of said daughter printed wiring board.

2. The apparatus of Claim 1, further comprising:

a connector comprising a plurality of electrical connections to said plurality of electrical conductors on said upper surface of said daughter printed wiring board.

3. The apparatus of Claim 2, wherein said connector is a separable connector comprising a first connector half and a second connector half, said first connector half and said second connector half forming a removable mating connection between a plurality of electrical connections on said first half and a plurality of electrical connections on said second half, said plurality of electrical connections on first connector half connected to said each of said plurality of electrical conductors on said upper surface of said daughter printed wiring board.

4. The apparatus of Claim 3, wherein said separable connector is an area array connector.

5. The apparatus of Claim 2, wherein said connector is an interposer.

6. The apparatus of Claim 2, further comprising:

a probe card substrate having a top surface and a bottom surface, and a plurality of electrical conductors extending from said top surface to said bottom surface, said plurality of electrical conductors on said bottom surface of said probe

card substrate in electrical contact with said plurality of electrical connections on said connector; and

a mechanical connection between said daughter printed wiring board and said probe card substrate.

7. The apparatus of Claim 6, wherein said mechanical connection between said probe card substrate and said daughter printed wiring board comprises at least one fastener assembly comprising a fastener and a fastener standoff.

8. The apparatus of Claim 7, wherein said mechanical connection is an adjustable mechanical connection.

9. The apparatus of Claim 6, wherein said connector is a separable connector comprising a first connector half and a second connector half, said first connector half and said second connector half forming a removable mating connection between a plurality of electrical connections on said first half and a plurality of electrical connections on said second half, said plurality of electrical connections on first connector half connected to said each of said plurality of electrical conductors on said upper surface of said daughter printed wiring board, and said plurality of electrical connections on said second connector half connected to each of said electrical conductors on said probe card substrate.

10. The apparatus of Claim 9, wherein said separable connector is an area array connector.

11. The apparatus of Claim 1, wherein said plurality of spring probe contact tips on said probe surface of said substrate are photolithographically patterned springs.

12. The apparatus of Claim 1, wherein each of said plurality of electrical connections between said plurality of electrically conductive pads and said plurality of electrical conductors on said bottom surface of said daughter printed wiring board are solder ball connections.

13. The apparatus of Claim 1, wherein said plurality of electrical connectors between each of said plurality of said spring probe contact tips on said probe

surface of said substrate and each of said plurality of electrically conductive pads on said connector surface of said substrate comprise metalized vias.

14. The apparatus of Claim 1, wherein said substrate further comprises at least one insulated reference plane.

15. The apparatus of Claim 1, wherein said substrate is electrically insulative.

16. The apparatus of Claim 1, wherein said substrate is dielectric.

17. The apparatus of Claim 1, wherein said substrate is at least partially conductive.

18. The apparatus of Claim 1, further comprising:

at least one lower substrate standoff fixedly attached to said probe surface of said substrate.

19. The apparatus of Claim 1, further comprising:

a capacitor incorporated as an assembled component on said daughter printed wiring board.

20. The apparatus of Claim 1, further comprising:

a capacitor incorporated as an assembled component on said substrate.

21. The apparatus of Claim 20, wherein said capacitor is fabricated on said substrate.

22. The apparatus of Claim 20, wherein said substrate is comprised of silicon, and wherein said capacitor is fabricated within said substrate.

23. A tile array, comprising:

a tiling substrate having a width and a length and having a probe surface and a connector surface;

at least one probe contact area located on said probe surface of said tiling substrate, each of said probe contact areas having a plurality of electrically conductive spring probes; and

a plurality of electrical connections extending through said tiling substrate between each of said plurality of said spring probe contact tips and said connector surface.

24. The tile array of Claim 23, wherein each of said plurality of electrically conductive spring probes on said probe surface of said tiling substrate are photolithographically patterned springs.

25. The tile array of Claim 23, wherein said plurality of electrical connections extending through said tiling substrate between each of said plurality of said spring probe contact tips and said connector surface are metalized vias.

26. The tile array of Claim 23, wherein said tiling substrate further comprises at least one insulated reference plane.

27. The tile array of Claim 23, wherein said tiling substrate has a low thermal coefficient of expansion.

28. The tile array of Claim 23, wherein said at least one probe contact area is aligned along said probe surface.

29. The tile array of Claim 23, further comprising:

a plurality of ball grid array solder connections on said connector surface of said tiling substrate, each of said ball grid array solder connections connected to each of said plurality of electrical connections on said connector surface of said tiling substrate.

30. The tile array of Claim 23, wherein at least one of said plurality of probe contact areas is comprised of a plurality of contact regions aligned along said width and said length of said probe surface.

31. A tiled probe assembly for connection to at least one integrated circuit device on a wafer, comprising:

a plurality of tiling substrates having a width and a length, each having a probe surface and a connector surface;

a plurality of probe contact areas located on said probe surface of each of said plurality of tiling substrates, each of said probe contact areas having a plurality of electrically conductive spring probes;

a plurality of electrical connections extending through each of said substrates between each of said plurality of said electrically conductive spring probes and said connector surface; and

a probe card substrate having a first surface and a second surface and a plurality of electrically conductive vias between said first surface and said second surface;

whereby each of said plurality of tiling substrates are positioned on said first surface of said probe card substrate, and whereby each said plurality of electrical connections are connected to each of said plurality of electrically conductive vias.

32. The tiled probe assembly of Claim 31, wherein said probe card substrate is comprised of a material having a similar thermal coefficient of expansion to said wafer.

33. The tiled probe assembly of Claim 31, wherein each of said plurality of tiling substrates provides a plurality of electrical connections to a single of said least one integrated circuit device through said plurality of electrically conductive spring probes.

34. The tiled probe assembly of Claim 31, wherein each of said plurality of tiling substrates provides a plurality of electrical connections to a plurality of said integrated circuit devices through said plurality of electrically conductive spring probes.

35. The tiled probe assembly of Claim 31, wherein said plurality of tiling substrates provides a plurality of electrical connections to said at least one integrated circuit device through said plurality of electrically conductive spring probes.

36. The tiled probe assembly of Claim 31, wherein each of said plurality of tiling substrates has a low thermal coefficient of expansion.

37. The tiled probe assembly of Claim 31, wherein each of said probe contact areas for each of said plurality of tiling substrates is aligned along said length of each of said probe surfaces.

38. The tiled probe assembly of Claim 31, further comprising:

a plurality of ball grid array solder connections on said connector surface of each of said plurality of tiling substrates, in which each of said ball grid array solder connections is connected to each of said plurality of electrical connections.

39. The tiled probe assembly of Claim 31, wherein each of said plurality of probe contact areas is comprised of a plurality of contact regions aligned along said probe surface.

40. A burn-in apparatus for at least one electrical device, comprising:

a burn-in board substrate having a first surface and a second surface, and a plurality of electrical conductors extending from said first surface to said second surface;

at least one contactor chip substrate having a connection surface, a probe contact surface, a plurality of flexible electrically conductive probe spring tips extending from said probe contact surface, and a plurality of electrical connections extending through each of said at least one said contactor chip substrate between each of said plurality of said flexible electrically conductive probe spring tips and said connector surface; and

a plurality of electrical connections between each of said plurality of electrical conductors on said second surface of said burn-in board substrate and each of said plurality of said electrical contacts on said connection surface of each of said at least one said contactor chip substrate.

41. The burn-in apparatus of Claim 40, wherein said plurality of flexible electrically conductive probe spring tips are photolithographically patterned springs.

42. The burn-in apparatus of Claim 40, wherein each of said plurality of electrical connections between each of said plurality of electrical conductors on said second

surface of said burn-in board substrate and each of said plurality of said electrical contacts on said connection surface of each of said at least one said contactor chip substrate is a solder ball connection.

43. The burn-in apparatus of Claim 40, wherein a board vacuum port is defined between said first surface and said second surface of said burn-in board substrate, and wherein a connector vacuum port is defined between said connection surface and said probe contact surface of said contactor chip substrate, whereby said board vacuum port and said connector vacuum port are generally aligned, such that an external vacuum applied to said board vacuum port at said first surface of said burn-in board substrate is also applied to said connector vacuum port of said contactor chip substrate.

44. The burn-in apparatus of Claim 43, further comprising:

an air seal defined between said second surface of said burn-in board substrate and said connection surface of said contactor chip substrate.

45. The burn-in apparatus of Claim 40, wherein each of said plurality of electrical connections are micro ball grid array connections.

46. The burn-in apparatus of Claim 40, further comprising:

a clamp plate adapted to hold said electrical device against said plurality of flexible electrically conductive probe spring tips extending from said probe contact surface of said contactor chip substrate.

47. The burn-in apparatus of Claim 46, further comprising:

at least one spring pad located between each of said at least one electrical device and said clamp plate.

48. A process, comprising the steps of:

providing a first substrate having a first surface and a second surface, said second surface having at least one non-planar conductive probe spring extending therefrom, said at least one non-planar conductive probe spring including a probe tip;

applying an electrically conductive coating to said second surface of said first substrate and said at least one non-planar conductive probe spring;

establishing a masking material on at least said probe tip of said at least one non-planar conductive probe spring;

curing said established masking material;

etching said coated and cured masked substrate to substantially remove portions of said electrically conductive coating which are not protected by said cured masking material; and

stripping said cured masking material from said substrate assembly.

49. The process of Claim 48, wherein said at least one non-planar conductive probe spring is formed by sputter deposition.

50. The process of Claim 48, wherein said at least one non-planar conductive probe spring is formed by a photolithographic process.

51. The process of Claim 48, wherein said electrically conductive coating comprises titanium nitride.

52. The process of Claim 48, wherein said electrically conductive coating comprises rhodium.

53. The process of Claim 48, wherein said electrically conductive coating comprises palladium.

54. The process of Claim 48, wherein said electrically conductive coating comprises tungsten.

55. The process of Claim 48, wherein said electrically conductive coating comprises nickel.

56. The process of Claim 48, wherein said electrically conductive coating comprises beryllium copper.

57. The process of Claim 48, wherein said electrically conductive coating is an inert coating.

58. The process of Claim 48, wherein said electrically conductive coating is resistant to galling.

59. The process of Claim 48, wherein said electrically conductive coating is resistant to oxidation.

60. The process of Claim 48, wherein said step of curing said established masking material is provided by baking said first substrate.

61. The process of Claim 48, wherein said step of establishing a masking material on at least said probe tip of said at least one non-planar conductive probe spring further comprises the steps of:

establishing a layer of said masking material on a second planar substrate; and

partially and controllably dipping said at least one non-planar conductive probe spring on said first substrate into said established layer of said masking material.

62. The process of Claim 60, wherein said second planar substrate further comprises at least one dipping standoff.

63. The process of Claim 48, wherein said step of establishing a masking material on said at least said probe tip of said at least one non-planar conductive probe spring further comprises the steps of:

establishing a layer of said masking material on a cylindrical roller;

providing a means for positioning said cylindrical roller at a controlled distance from said second surface of said first substrate; and

rolling said cylindrical roller across said positioning means to establish said masking material on said at least said probe tip of said at least one non-planar conductive probe spring.

64. The process of Claim 48, wherein said masking material comprises photoresist.

65. The process of Claim 64, wherein said photoresist is approximately 10 microns deep.

66. The process of Claim 48, wherein said masking material comprises silicone.

67. The process of Claim 48, wherein said masking material comprises wax.

68. The process of Claim 48, wherein said masking material comprises epoxy.

69. The process of Claim 48, wherein said etching step comprises ion milling.

70. The process of Claim 48, further comprising the steps of:

applying a hard mask to said second surface of said first substrate and said at least one non-planar conductive probe spring after said step of applying said electrically conductive coating; and

removing said applied hard mask from said second surface of said first substrate and said at least one non-planar conductive probe spring to substantially remove portions of said hard mask which are not protected by said masking material, after said step of establishing said masking material on at least said probe tip of said at least one non-planar conductive probe spring.

71. The process of Claim 70, further comprising the step of:

removing said established masking material from each of said at least one said probe tip of said at least one non-planar conductive probe spring, after said removing of said hard mask.

72. The process of Claim 70, wherein said removing of said hard mask is provided by etching said applied hard mask from said second surface of said first substrate and said at least one non-planar conductive probe spring to substantially remove portions of said hard mask which are not protected by said masking material.